Remarks

In the Office Action, the Examiner noted that claims 1-38 are pending in the application, and that claims 1-38 are rejected. By this amendment, claims 3-4, 7-11, 14-18, and 36-38 have been canceled, and claims 1-2, 5-6, 13, 25, and 29 have been amended. Thus, claims 1-2, 5-6, 12-13, and 19-35 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

The Examiner objected to the disclosure. Applicant has filled in the serial numbers of the co-pending applications on page 1 as required by the Examiner. Applicant has also amended the summary as required by the Examiner.

The Examiner objected to claim 1 because of informalities. Claim 1 has been amended as requested by the Examiner.

The specification has also been amended to insert the patent numbers of issued U.S. patents incorporated by reference in the specification.

In the Claims

Rejection Under 35 USC 102(b)

The Examiner rejected claims 1-7, 10-16, and 18-36 under 35 U.S.C. § 102(b), as being anticipated by *Shiell et al.*, U.S. Patent No. 5,850,543 (hereinafter *Shiell*). Applicant respectfully traverses with respect to claims 1-2, 5-6, 12-13, and 19-35.

With respect to claim 1, the Examiner asserts that *Shiell* teaches a BTAC configured to provide a plurality of cached target addresses and offsets associated with a plurality of previously executed branch instructions in response to an instruction cache fetch address, and inherently teaches branch control logic that selects one of the plurality of target addresses provided by the BTAC as a subsequent fetch address in response to the fetch address and offsets, citing *Shiell*'s branch target buffer (BTB). Applicant respectfully asserts that *Shiell* does not teach, explicitly or inherently, a BTAC configured to provide

a plurality of cached target addresses and offsets indexed by an instruction cache fetch address, where the target addresses and offsets are associated with a plurality of previously executed branch instructions in a cache line selected by the fetch address, and branch control logic that selects one of the plurality of target addresses as a subsequent fetch address in response to the fetch address and offsets, as recited in amended claim 1. *Shiell*'s BTB is a memory arranged as a cache-like configuration. Col. 8, lines 22-24. As may be seen from Fig. 2, *Shiell*'s BTB is arranged as an array of entries indexed by a fetch address used to select an instruction code line. As shown in Fig. 3, each entry in *Shiell*'s BTB includes a tag of a previously taken branch instruction. If the fetch address matches one of the tags, the BTB provides the entry associated with the matching tag. Each entry also includes a target address and an offset indicating the starting offset of the specific branch instruction within the instruction code line associated with the tag. However, *Shiell*'s BTB does not include an entry for a plurality of previously taken branch instructions within the instruction code line associated with the tag, therefore *Shiell*'s BTB cannot and does not provide a plurality of target addresses and offsets that are selected based on the fetch address and offsets. In other words, *Shiell*'s BTB can only predict a single branch instruction within a given cache line fetched from the instruction cache. In contrast, Applicant's invention recited in claim 1 is capable of providing a prediction for one of a plurality of branch instructions within a given cache line fetched from the instruction cache.

Applicant notes that *Shiell* teaches one embodiment in which his BTB comprises a 4-way set associative cache. Hence, the fetch address may select four target address/offset pairs for four different branch instructions in the BTB. However, according to the properties of set associative caches, the four different branch instructions will be in different instruction cache lines, not the same instruction cache line.

For the reasons stated above, Applicant respectfully asserts that *Shiell* does not anticipate claim 1.

Applicant respectfully asserts that *Shiell* does not anticipate independent claims 13, 25, or 29 as amended for the reasons discussed above with respect to claim 1, because those claims recite similar limitations to claim 1 which are not taught by *Shiell.*

Applicant respectfully asserts that *Shiell* does not anticipate dependent claims 5-6, 19-24, 26-28, and 30-35 because they depend from independent claims 1, 13, 25, and 29, respectively, which are not anticipated by *Shiell* for the reasons discussed above.

The Examiner has indicated additional prior art which is made of record and not relied upon. None of these references anticipate or obviate applicant's invention.

For all of the reasons advanced above, Applicant respectfully submits that claims 1-2, 5-6, 12-13, and 19-35 are in condition for allowance. Reconsideration of the rejections is requested, and Allowance of the claims is solicited.

Applicant earnestly requests the Examiner to telephone him at the direct dial number printed below if the Examiner has any questions or suggestions concerning the application or allowance of any claims thereof.

Respectfully submitted,

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"EXPRESS MAIL" mailing label number EO002029165US Date of Deposit 6-8-04. I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 C.F.R. §1.10 on the date shown above and is addressed to the U.S. Commissioner of Patents and Trademarks, Alexandria, VA, 22313.

By: Vicki J. Hoge